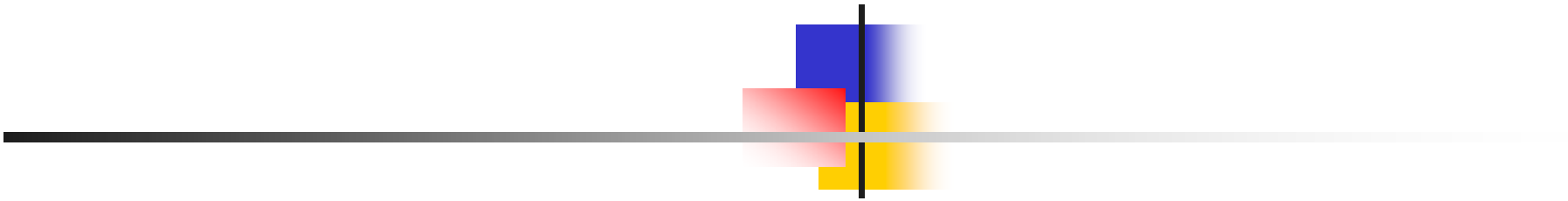
CSE398: Network Systems Design



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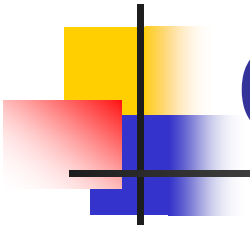
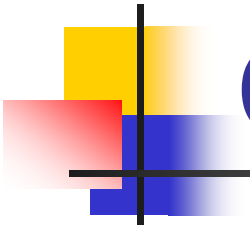


Outline

- Recap
  - Examples of commercial network processors
  - Design tradeoffs and consequences
- Overview of Agere's network processor
- Functional units on APP550
- Summary and homework



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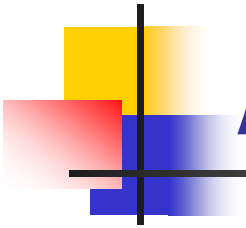
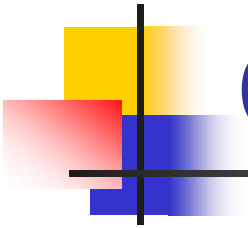
Agere PayloadPlus (APP)



- Architecture and technologies
  - Control plane and data plane processing
  - Defines:
    - Hardware, software, interconnection, and API
  - Does not specify an implementation
- APP refers to the 2nd generation chips
  - Number, type of functional units
  - Degree of processing parallelism
  - Internal data bandwidth

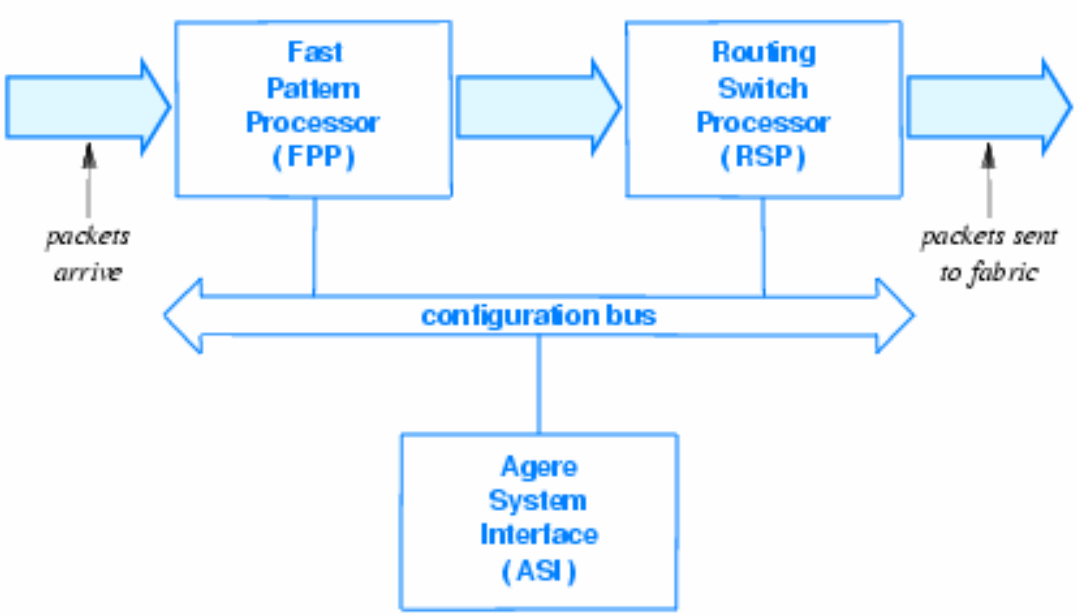
Conceptual Pipeline

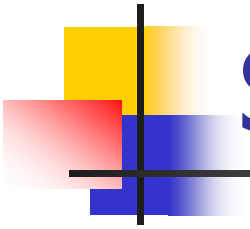


- Packet classification -> forwarding
  - Error checking
  - Classification
  - Statis. to state engine
  - Results to forwarder
  - traffic management
  - queueing
  - fragmentation
  - header modification
- Placed b/w a NIC and a switching fabric

First Generation

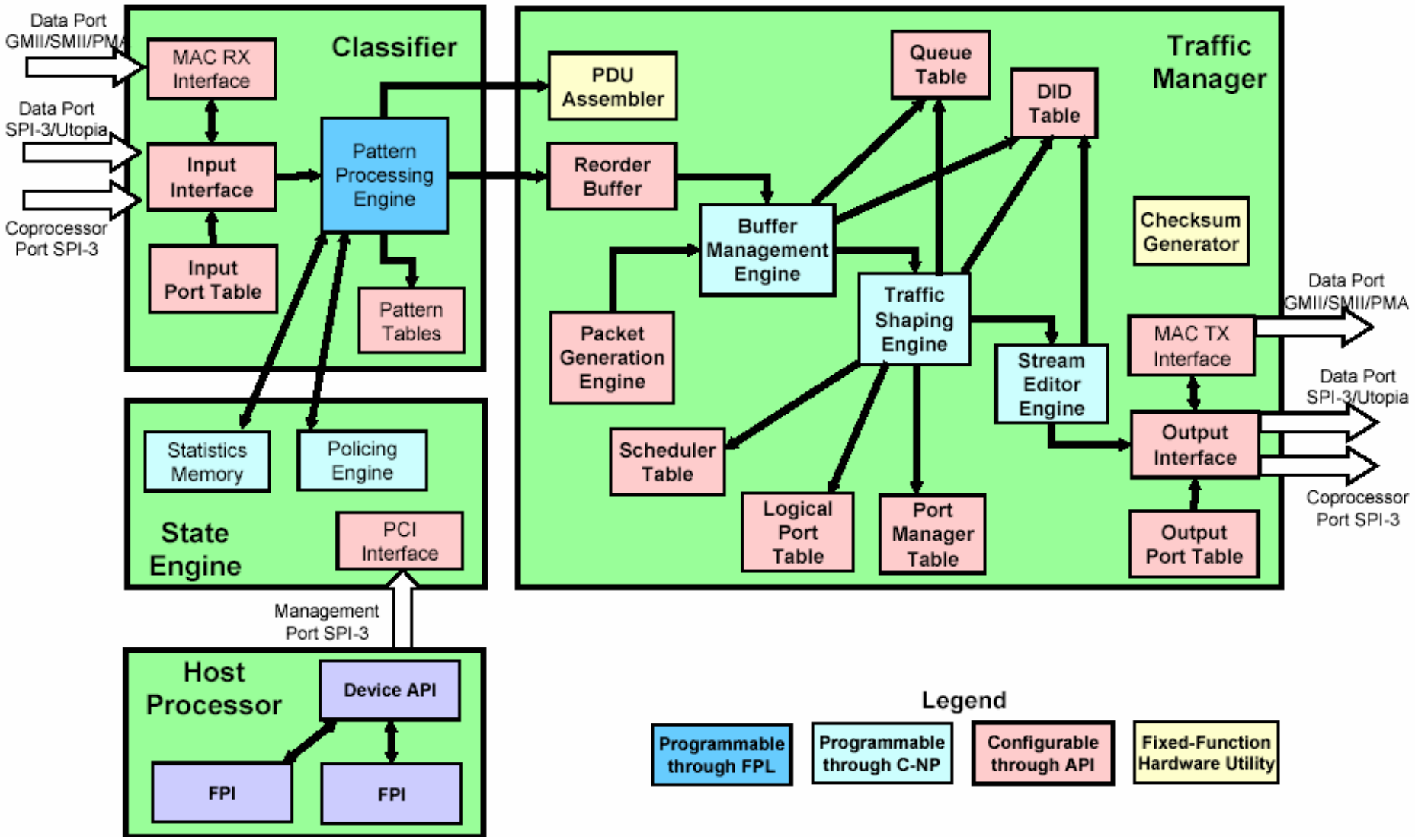
- Three separate chips
- FPP+RSP: fast path of data plane
- ASI: statistics, interface to a host microprocessor for system mgmt.



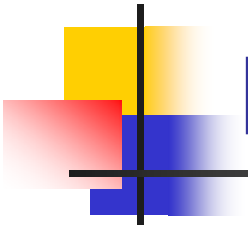


Second Generation

- A single IC but various models
  - APP550: four GigE ports with full capability
    - Classification: pattern processor
    - Forwarding: traffic manager and modifier
    - Statistics and host communication: state engine

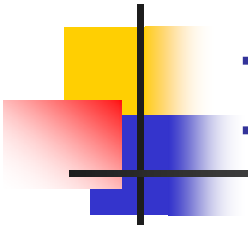

Data Port GMII/SMII/PMA
Data Port SPI-3/Utopia
Coprocessor Port SPI-3
MAC RX Interface
Classifier
Input Interface
Pattern Processing Engine
Input Port Table
Pattern Tables
Statistics Memory
Policing Engine
State Engine
PCI Interface
Management Port SPI-3
Host Processor
Device API
FPI
FPI
PDU Assembler
Reorder Buffer
Queue Table
DID Table
Traffic Manager
Buffer Management Engine
Checksum Generator
Packet Generation Engine
Traffic Shaping Engine
Stream Editor Engine
MAC TX Interface
Data Port GMII/SMII/PMA
Scheduler Table
Logical Port Table
Port Manager Table
Output Interface
Data Port SPI-3/Utopia
Output Port Table
Coprocessor Port SPI-3
Legend
Programmable through FPL
Programmable through C-NP
Configurable through API
Fixed-Function Hardware Utility

External Connections



- Memory interface
  - Fast cycle random access memory (FCRAM)
  - Double data rate static random acess memory (DDR-SRAM)
- Media interface
  - ATM and GigE
  - Standard interface: GMII, PMII, SMII, …
  - 64-byte blocks
- Switching fabric interface
  - Standard SPI-3 (System packet interface level 3)
- PCI bus interface
  - To GPP host processor
- Scheduling interface
- Coprocessor interface: SPI-3

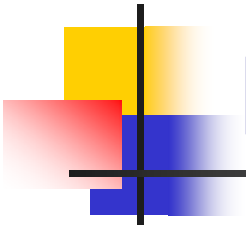
Internal Architecture



- Engines
  - Pattern processing engine: classification
  - State engine: state info for scheduling and verifying flow is within bound
  - Reorder buffer manager: ensure packet order
  - PDU assembler: collect blocks of a frame
  - Traffic manager: schedule packets and shape traffic flow
  - Stream editor: modify outgoing packets

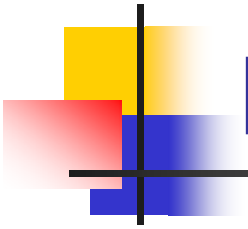
Engine Functionality

- Engines
  - Pattern processing engine
  - State engine
  - Reorder buffer manager
  - PDU assembler
  - Traffic manager
  - Stream editor
- Schedule output queues based on time, congestion, priorities, flags
- Enqueue or discard an outgoing PDU
- Fragment and/or modify PDUs and update checksums before transmission



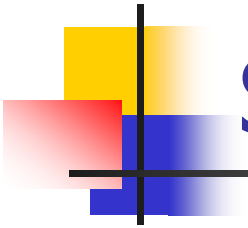
Pattern Processing Engine (1)

- Programmers specify a set of patterns
  - Programmable: FPL -> compilation -> PPE
  - Unconventional: pattern matching
  - Implicit parallelism
  - Automatic invocation
  - Transparent access to multiple memories
    - Classifier PDU buffer
    - Classifier program memory
    - Classifier control memory



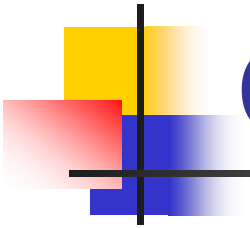
Pattern Processing Engine (2)

- Data flow through the classifier
  - Ingress storage
  - First pass of classification
  - Second pass of classification
  - Reassembly and handoff



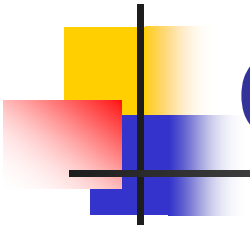
Stream Editor

- Fast path
- Two identical copies
  - Create up to 127 bytes of frame header
  - Fragmentation
  - Create up to 20 bytes of cell header
  - Modification
  - Encapsulate the packet
  - Control CRC hardware and append results



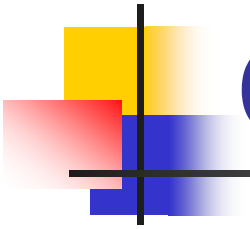
Global Pulse

- Pipeline architecture
  - Each stage must complete before the next packet arrives
  - Global pulse specifies the amount of time available to process a packet
    - For an OC-48 (2.5 Gbps) interface: 23 instructions
    - Programmer should guarantee that no engine runs for more than the global pulse



Other Functional Units

- Packet generation engine
  - ATM's operation, administration, and maintenance (OAM)
  - ICMP packets



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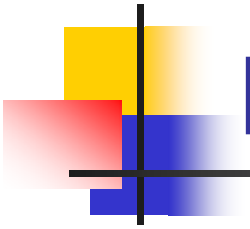
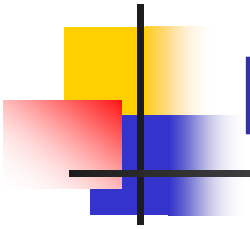


Review Question

- Page 266 Exercise 17.3: What is the advantage of separating classification from forwarding?



Homework (due 04/11)

- 11.1. (a) Problem 1 of Chapter 17; (b) Problem 2 of Chapter 17. (Page 266)