CSE398: Network Systems Design

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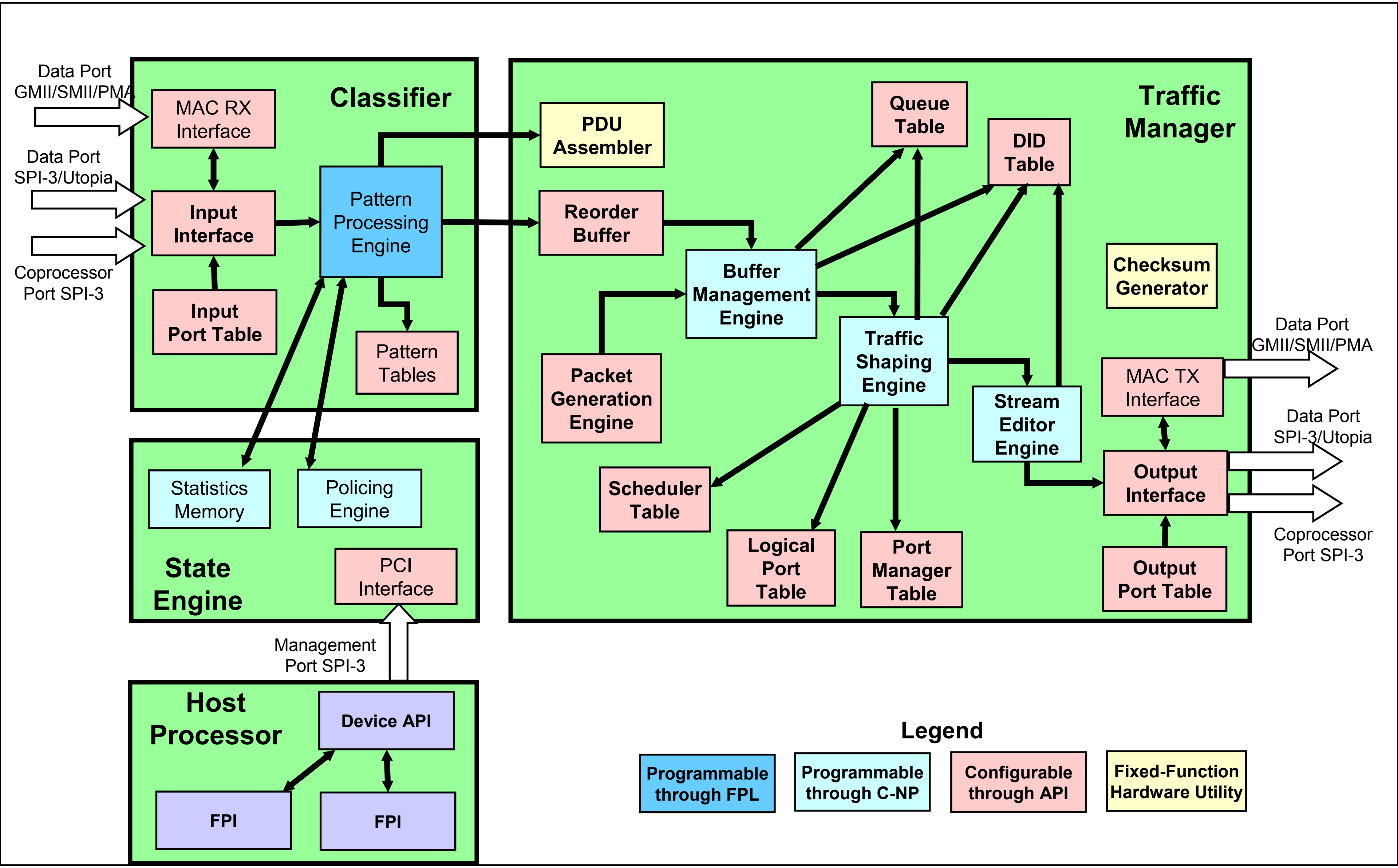
Outline

- Recap
  - APP550 network processor architecture
- SPA and FPL classification language
- Summary and homework

Summary of NP Functions

- Routing
  - **Where to send frame/cell/packet (network/node/app).**
- Modification
  - **Fragmentation / reassembly, compression / decompression, encryption / decryption, encapsulation / decapsulation (tunneling).**
- Traffic management and shaping
  - **Packet discard and traffic buffering/smoothing, based on policies, time, congestion, priority, resources.**
- Enterprise applications
  - **Firewall/VPN, NAT, ALG, load balancing, storage area networks (SAN), layer 4-7 packet processing.**

APP550 Overview



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FPL: Application Oriented Language (AOL)

- AOLs enhance expressiveness within a domain, without a loss in efficiency, costing generality.
- Compilation and hardware architecture optimize application processing.
- Manage complexity by eliminating accidental complexity, focusing on essential complexity.
- Examples
  - AWK for text processing
  - SQL for database interaction
  - Graphics languages
- FPL is an AOL for classification. FPL uses pattern matching supported by APP550.
- Function call syntax for language generality.

An FPL Example

- Examine README.txt and .fpl files in examples/webbump on CD.
- This example sends traffic to the opposite output port, counting packets destined for TCP port 80 (web server).

FPL Tree Functions

- Variants of a given tree function must match identical number of bits.
- A variant matches a distinct pattern of constants followed by wildcards.
- BITS:n is the all wildcard, default case.
- Selection is by most specific leading match (longest prefix matching).
- Slow path microprocessor can learn tree patterns, e.g., for compiling route tables at run time.

Example Tree Function Patterns

- matchtest: 192.19.194.178
  // procedural "flow instructions" go here
  ;
- matchtest: 192:8 19:8 194:8 BITS:8
  // same as 192.19.194.*
- matchtest: 192.19.*.*
- matchtest: 192.*.*.*
- matchtest: 192:8 19:8 RANGE(179,185):8 BITS:8
- matchtest: BITS:32 // default catch-all

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Summary

- FPL provides two-pass, assemble and match processing.
- Classification engine uses multi-bit FPL tree instructions to match data.
- Slow path microprocessor can learn tree patterns such as route tables at run time.
- Flow instructions include arithmetic, logic, fetch/store, branching.
- C-NP engines maintain policing state and process traffic flow.

Self-study Materials (1)

- Read “Introduction” through “Using Global Registers” (under “Understanding and Using FPL Programming Concepts”) in the FPL User’s Guide (FPL-Users-Guide.pdf).
- Examine “Common Functions” and “Functions Available to the APP500 Chip Family” in the FPL Reference Guide (FPL-Ref-Guide.pdf), especially fExtract, fSkip, fReturn, fQueue, fQueueEOF, and fTransmit.

Self-study Materials (2)

- Read “Overview” through “Classifier” under “How the APP550/530 Works” in Technical Guide to the APP550 and APP530 Network Processors (APP550_530_20050125.pdf).
- Examine README.txt and .fpl files in labs/example4_fpl_webbump and labs/lab4_fpl_ethbridge_2003.