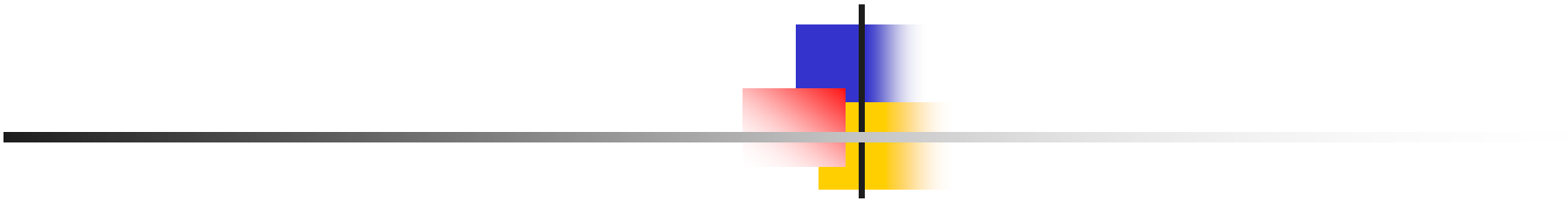
CSE398: Network Systems Design



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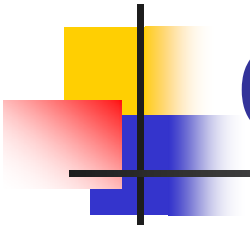
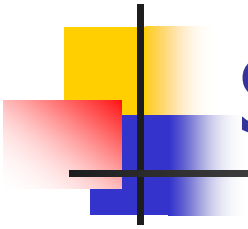


Outline

- Recap
  - TCP, UDP, application layer protocols
- Computer hardware architecture
- Summary and homework

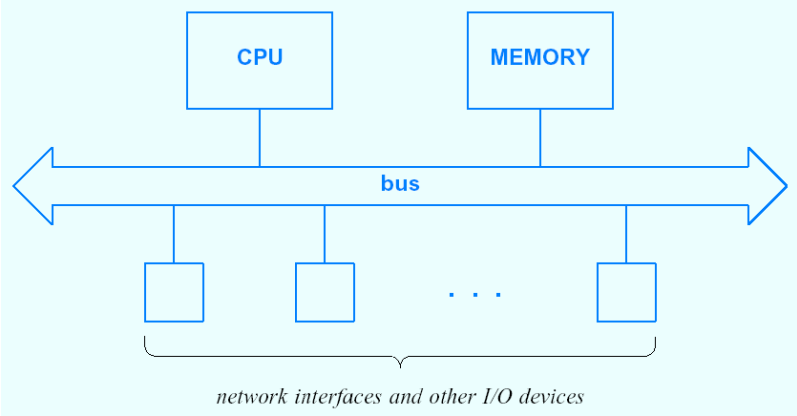


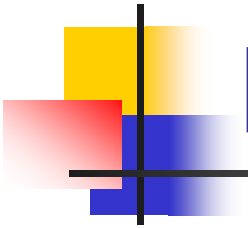
Software-based Network System

- Uses conventional hardware (e.g., PC)
  - CPU, memory, bus, I/O devices
- Software
  - Runs the entire system
  - Allocates memory
  - Controls I/O devices
  - Performs all protocol processing

Bus

- Bus: b/w I/O and CPU & Memory
  - All components contend for use
- Parallel wires (K+N+C total)
  - An address of K bits
  - A data value of N bits (width of the bus)
  - Control information of C bits
- Wider bus
  - Transfers more data per unit time
  - Costs more
  - Requires more physical space
  - Compromise: multiplex



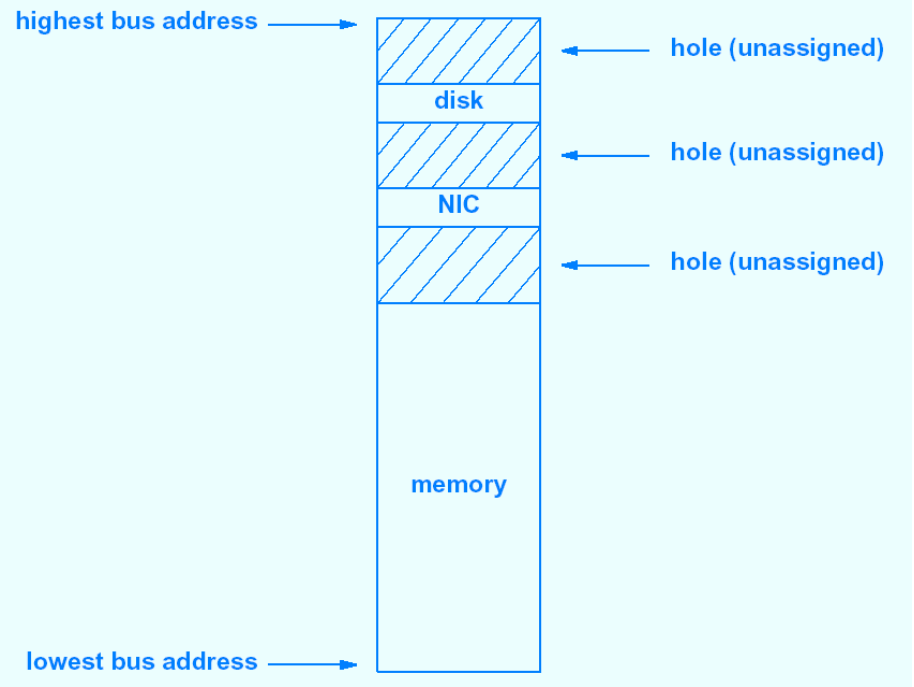


Fetch and Store

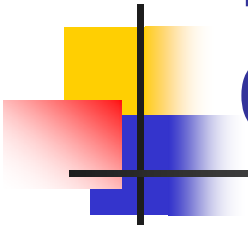
- Fundamental paradigm
  - Used throughout hardware (network processor)
- Fetch operation
  - Place address of a device on address lines
  - Issue fetch on control lines
  - Wait for device that owns the address to respond
  - If successful, extract value (response) from data lines
- Store operation
  - Place address of a device on address lines
  - Place value on data lines
  - Issue store on control lines
  - Wait for device that owns the address to respond
  - If unsuccessful, report error

Bus Address Space

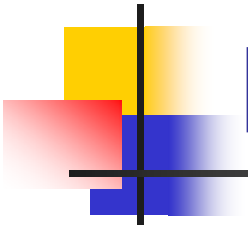
- Arbitrary hardware can be attached to bus
- *K* address lines result in 2^k possible bus addresses
- Address can refer to
  - Memory (e.g., RAM or ROM)
  - I/O device
- Arbitrary devices can be placed at arbitrary addresses
- Address space can contain "holes"
- Device on bus known as *memory mapped I/O*
- Locations that correspond to nontransfer operations known as *Control and Status Registers* (CSRs)



Network I/O on Conventional Hardware

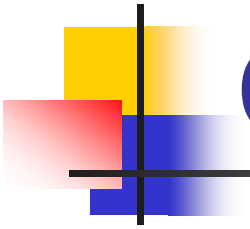


- Network Interface Card (NIC)
  - Attaches between bus and network
  - Operates like other I/O devices
  - Handles electrical/optical details of network
  - Handles electrical details of bus
  - Communicates over bus with CPU or other devices



NIC Functionality

- Onboard address recognition and filtering
- Onboard packet buffering
- Direct memory access (DMA)
- Data chaining and operation chaining



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Homework (due on 02/07)

- 4.1. Describe (a) what is an IP multicast address? (b) what is a MAC multicast address? (c) and how an IP multicast address be mapped to a corresponding MAC address. Hint: read related info at http://netweb.usc.edu/multicast/ and search WWW for the sub-question (c).

- Questions NOT for hand-in: Read Chapter 1 to Chapter 5, especially algorithms in Chapter 5.