CSE398: Network Systems Design

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February 7, 2005
Outline

- Recap
  - Computer hardware architecture
  - Fetch and store
- Packet processing algorithms (Chapter 5)
- Summary and homework
NIC Functionality

- Onboard address recognition and filtering
- Onboard packet buffering
- Direct memory access (DMA)
- Data chaining and operation chaining
Onboard Address Recognition And Filtering

- NIC given set of addresses to accept
  - Station’s unicast address
  - Network broadcast address
  - Zero or more multicast addresses (≤32 or 64)
    - CPU must be prepared to handle a false acceptance

- When packet arrives, NIC checks destination address
  - Accept packet if address on list
  - Discard others
Onboard Packet Buffering

- NIC given high-speed local memory
- Incoming packet placed in NIC’s memory
  - Allows computer’s memory/bus to operate slower than network
  - Handles small packet bursts
Direct Memory Access (DMA)

- **CPU**
  - Allocates packet buffer in memory
  - Passes buffer address to NIC
  - Goes on with other computation

- **NIC**
  - Accepts incoming packet from network
  - Copies packet over bus to buffer in memory
  - Informs CPU that packet has arrived
Buffer/Data Chaining

- CPU
  - Allocates multiple buffers
  - Passes linked list to NIC

- NIC
  - Receives next packet
  - Divides into one or more buffers

- Advantage: a buffer can be smaller than packet
Operation/Command Chaining

- CPU
  - Allocates multiple buffers
  - Builds linked list of operations
  - Passes list to NIC

- NIC
  - Follows list and performs instructions
  - Interrupts CPU after each operation

- Advantage: multiple operations proceed without CPU intervention
Data Flow Diagram

- Depicts flow of data through hardware units
- Used throughout the course and text
Outline

- Today’s class ends at 1:55 PM
- Recap
  - Packet processing algorithms (Chapter 5)
    - Data storage and representation
    - Algorithms
- Summary and homework
Why Study Packet Processing on Conventional Hardware?

- **Past**
  - Employed in early IP routers
  - Many algorithms developed / optimized for conventional hardware

- **Present**
  - Used in low-speed network systems
  - Easiest to create / modify
  - Costs less than special-purpose hardware

- **Future**
  - Processors continue to increase in speed
  - Some conventional hardware present in all systems
Copying and Buffering

- Used when packet moved from one memory location to another
  - Expensive
- Must be avoided whenever possible
  - Leave packet in buffer
  - Pass buffer address among threads/layers
- Buffer allocation
  - Large, fixed buffers
  - Variable-size buffers
  - Linked list of fixed-size blocks
Integer Representation

- Little endian (least-significant byte at lowest address): Intel 80x86
- Big endian (most-significant byte at lowest address): Motorola 680x0
- Integer conversion
  - Needed when heterogeneous computers communicate
  - Protocols define network byte order: big-endian
  - Computers convert to network byte order

<table>
<thead>
<tr>
<th>Function</th>
<th>data size</th>
<th>Translation</th>
</tr>
</thead>
<tbody>
<tr>
<td>ntohs</td>
<td>16 bits</td>
<td>Network byte order to host’s byte order</td>
</tr>
<tr>
<td>htons</td>
<td>16 bits</td>
<td>Host’s byte order to network byte order</td>
</tr>
<tr>
<td>ntohl</td>
<td>32 bits</td>
<td>Network byte order to host’s byte order</td>
</tr>
<tr>
<td>htonl</td>
<td>32 bits</td>
<td>Host’s byte order to network byte order</td>
</tr>
</tbody>
</table>
Algorithm Examples

- Layer 2
  - Ethernet bridge
- Layer 3
  - IP forwarding
  - IP fragmentation and reassembly
- Layer 4
  - TCP connection recognition and splicing
- Other
  - Hash table lookup
Ethernet Bridge

- Used between a pair of Ethernets
- Provides transparent connection
- Listens in promiscuous mode
- Forwards frames in both directions
- Uses source address in frames to identify computers on each network
- Uses addresses to filter
  - Uses destination address to decide whether to forward frame
Learning Bridge Algorithm

Assume: two network interfaces each operating in promiscuous mode.
Create an empty list, L, that will contain pairs of values;
Do forever {
    Acquire the next frame to arrive;
    Set I to the interface over which the frame arrived;
    Extract the source address, S;
    Extract the destination address, D;
    Add the pair (S, I) to list L if not already present.
    If the pair (D, I) appears in list L {
        Drop the frame;
    } Else {
        Forward the frame over the other interface;
    }
}
Outline

- Recap
- Packet processing algorithms
- Summary and homework
Homework (due on 02/14)

5.1. Give the big-endian and little-endian representations of the integer 34677374.

5.2. Problem 2 of Chapter 5 (Page 63).