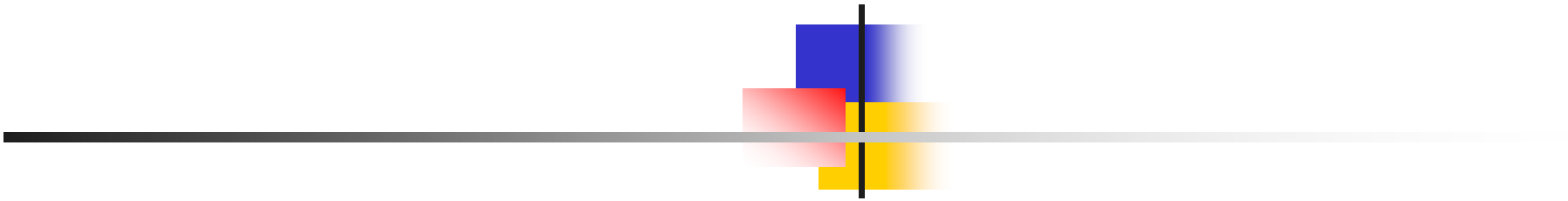
CSE398: Network Systems Design



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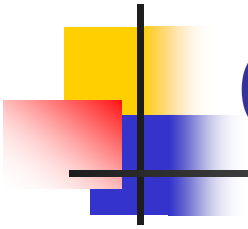
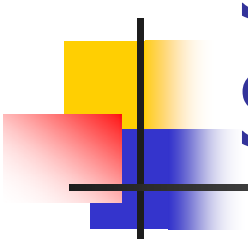
March 16, 2005



Outline

- Recap
  - Traditional protocol processing systems
  - Start Part II
- Second generation network systems
- Third generation network systems
- Fourth generation network systems
  - Network processor
- Summary and homework

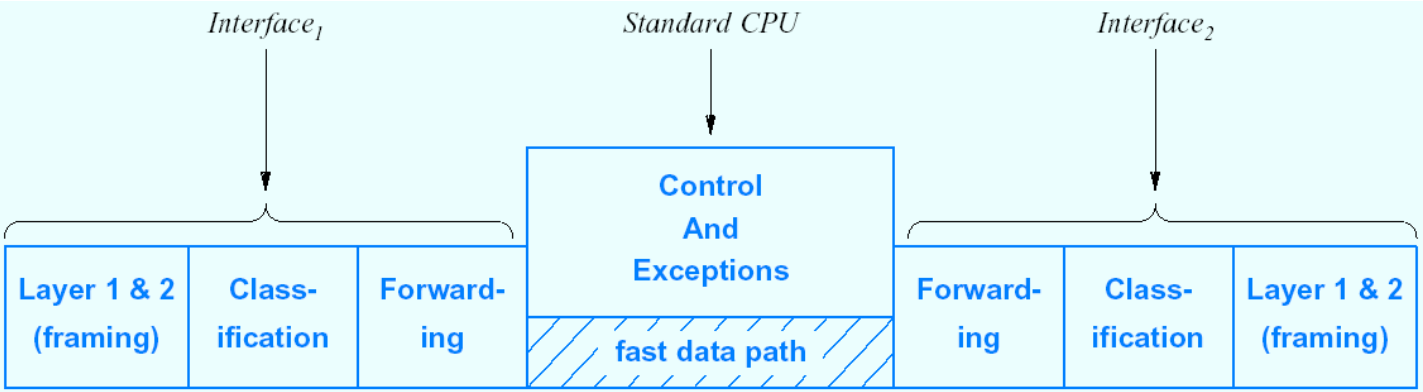
Second Generation Network Systems

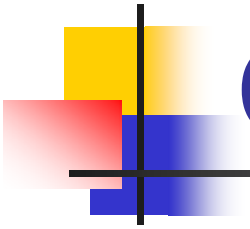


- Concurrent with ATM development (early 1990s)
- Purpose: scale to speeds faster than single CPU capacity
- Features
  - Use classification instead of demultiplexing
  - Decentralized architecture to offload CPU
  - Design optimized for fast data path

Second GNS Details

- Multiple network interfaces
  - Powerful NIC
  - Private buffer memory
- High-speed hardware interconnects NICs
- General-purpose processor only handles exceptions
- Sufficient for medium speed interfaces (100 Mbps)
- NIC handles most of layers 1 - 3
- Fast-path forwarding avoids CPU completely





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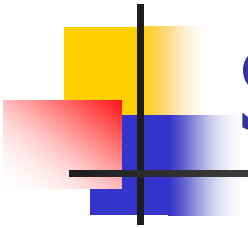
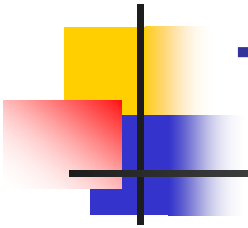
Third Generation Network Systems

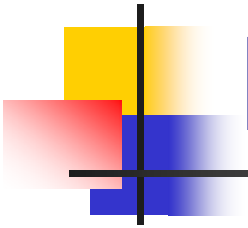


- Late 1990s
- Functionality gets partitioned further
- Additional hardware on each NIC
- Almost all packet processing off-loaded from CPU



Third Generation Design

- NIC contains
  - ASIC hardware
  - Embedded processor plus code in ROM
- NIC handles
  - Classification
  - Forwarding
  - Traffic policing
  - Monitoring and statistics

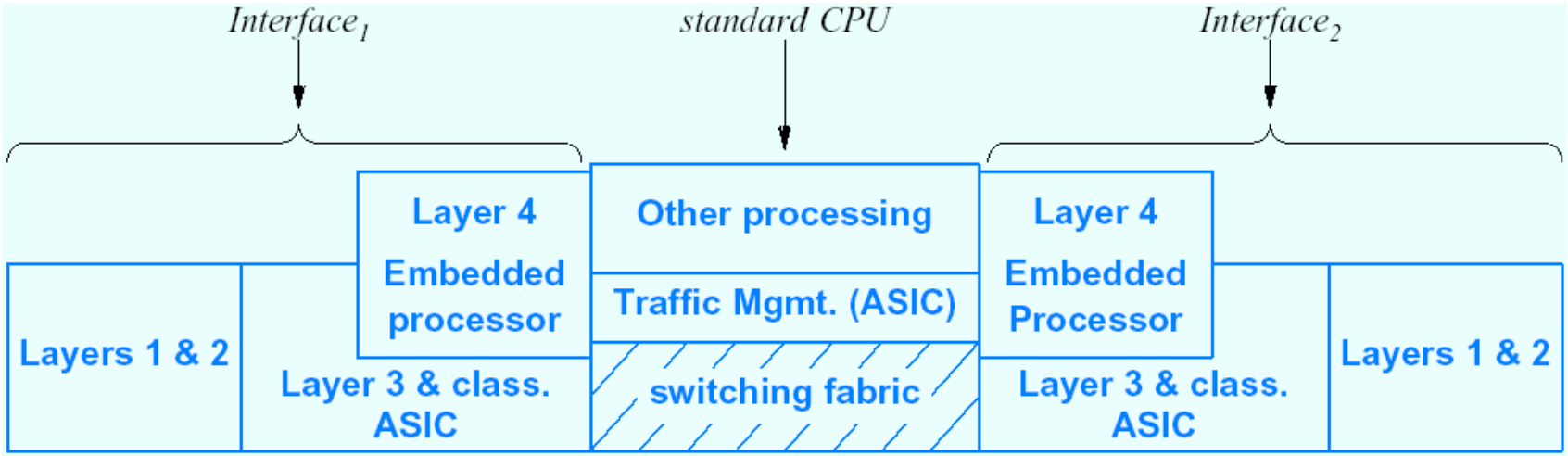


Embedded Processor

- Purpose
  - Handle layer 4 functionality & exception packets
  - Ease of implementation
  - Amenability to change
- Two possibilities
  - Complex Instruction Set Computer (CISC)
  - Reduced Instruction Set Computer (RISC)
- RISC used often because
  - Higher clock rates
  - Smaller
  - Lower power consumption

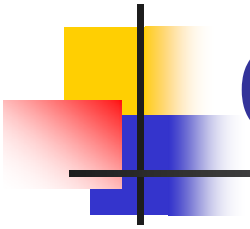
Protocol Processing in Third Generation Systems

- Special-purpose ASIC for lower layer functions
- Embedded (RISC) processor handles layer 4
- CPU only handles low-demand processing



Problems with Third Generation Systems

- High cost
- Long time to market
- Difficult to simulate/test
- Expensive and time-consuming to change
  - Even trivial changes require silicon respin
  - 18-20 month development cycle
- Little reuse across products
- Limited reuse across versions
- No consensus on overall framework
- No standards for special-purpose support chips
- Requires in-house expertise (ASIC designers)



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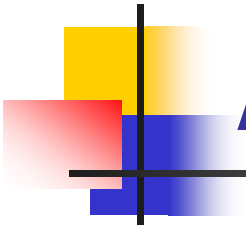
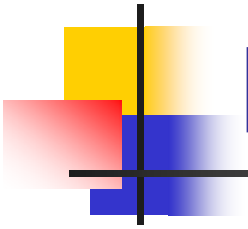
A Fourth Generation

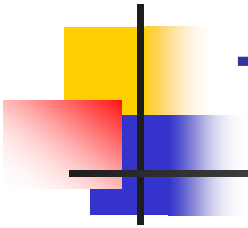


- Goal: combine best features of first, second generation and third generation systems
  - Flexibility of programmable processor
  - High speed of ASICs
- Technology called *network processors*
  - A network processor is a special-purpose, programmable hardware device that combines the low cost and flexibility of a RISC processor with the speed and scalability of custom silicon (i.e., ASIC chips). Network processors are building blocks used to construct network systems.



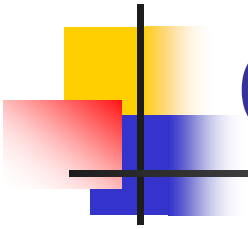
Potential Advantages

- Relatively low cost
- Straightforward hardware interface
- Facilities to access
  - Memory
  - Network interface devices
- Programmable
- Ability to scale to higher
  - Data rates
  - Packet rates



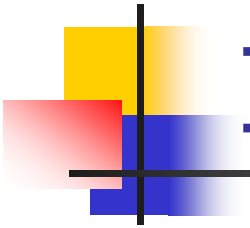
The Promise of Programmability

- For producers
  - Lower initial development costs
  - Reuse software in later releases and related systems
  - Faster time-to-market
  - Same high speed as ASICs
- For consumers
  - Much lower product cost
  - Inexpensive (firmware) upgrades



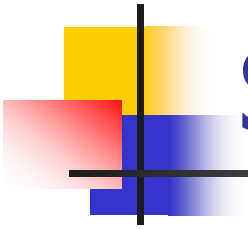
Choice of Instruction Set

- Programmability alone insufficient
- Also need higher speed
- Should network processors have
  - Instructions for specific protocols?
  - Instructions for specific protocol processing tasks?



Instruction Set

- Need to choose one instruction set
- No single instruction set best for all uses
- Other factors
  - Power consumption
  - Heat dissipation
  - Cost

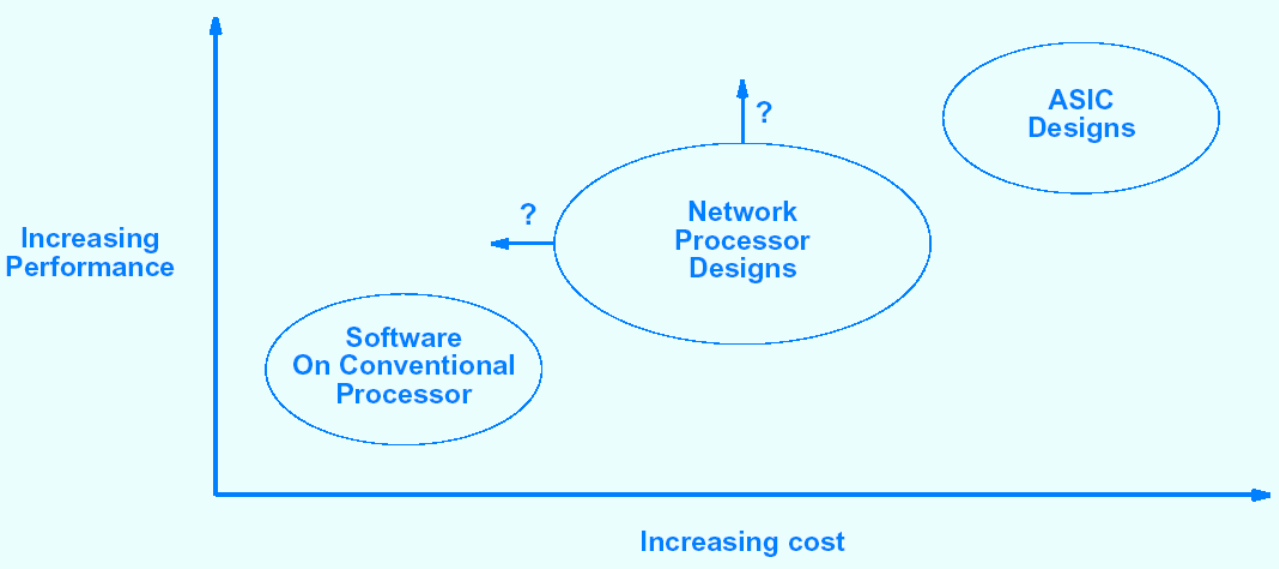


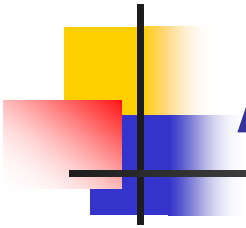
Scalability

- Two primary techniques
  - Parallelism
  - Data pipelining
- Questions
  - How many processors?
  - How should they be interconnected?

Costs and Benefits of Network Processors

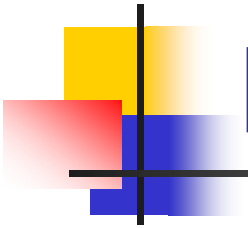
- Currently
  - More expensive than conventional processor
  - Slower than ASIC design
- Where do network processors fit?
  - Somewhere in the middle





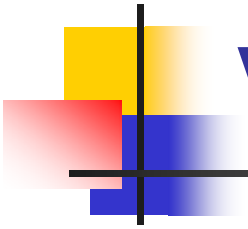
Achieving Higher Speed

- What is known
  - Must partition packet processing into separate functions
  - To achieve highest speed, must handle each function with separate hardware
- What is unknown
  - Exactly what functions to choose
  - Exactly what hardware building blocks to use
  - Exactly how building blocks should be interconnected



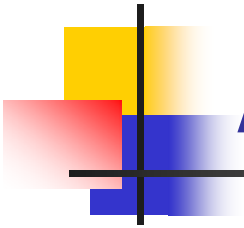
Functions We have Considered

- Address lookup and packet forwarding
- Error detection and correction
- Fragmentation, segmentation, & reassembly
- Frame and protocol demultiplexing
- Packet classification
- Queueing and packet discard
- Scheduling and timing
- Security: authentication and privacy
- Traffic measurement and policing
- Traffic shaping



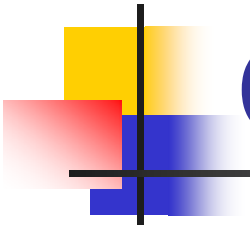
Variety of Network Processors

- Economics driving a gold rush
  - NPs will dramatically lower production costs for network systems
  - A good NP design potentially worth lots of $$
- Result
  - Wide variety of architectural experiments
  - Wild rush to try yet another variation



An Interesting Observation

- System developed using ASICs
  - High development cost ($1M)
  - Lower cost to replicate
- System developed using network processors
  - Lower development cost
  - Higher cost to replicate
- Conclusion: amortized cost favors ASICs for most high volume systems



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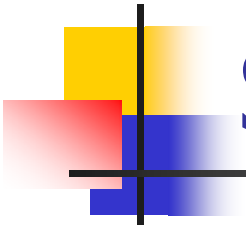

Summary

- Third generation network systems have embedded processor on each NIC
- Network processor is programmable chip with facilities to process packets faster than conventional processor
- Primary motivation is economic
  - Lower development cost than ASICs
  - Higher processing rates than conventional processor

Homework (Due March 21)

- 8.3. Problem 7 of Chapter 11 (page 171)
- Lab report of Lab#3 due on Mar. 23rd.