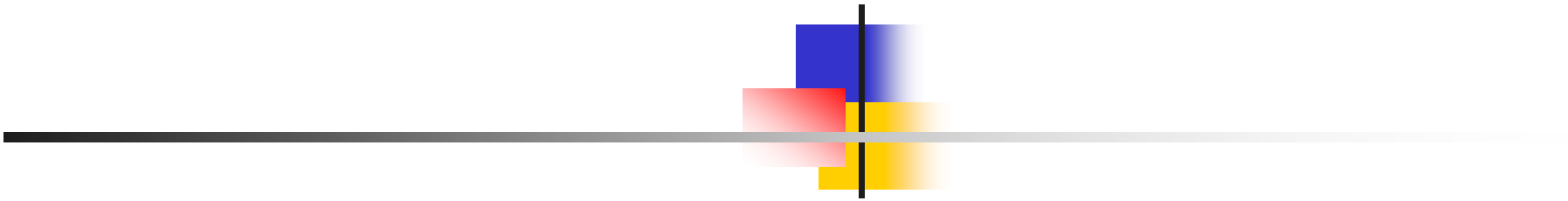
CSE398: Network Systems Design



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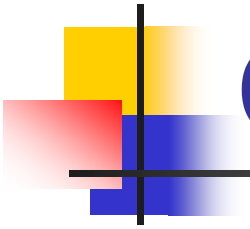
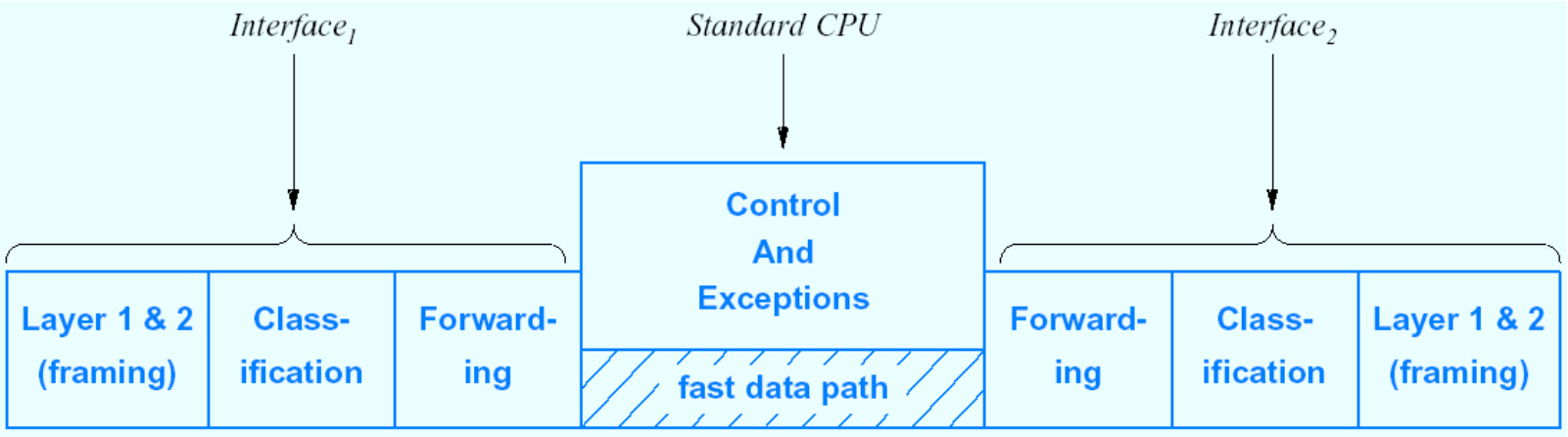
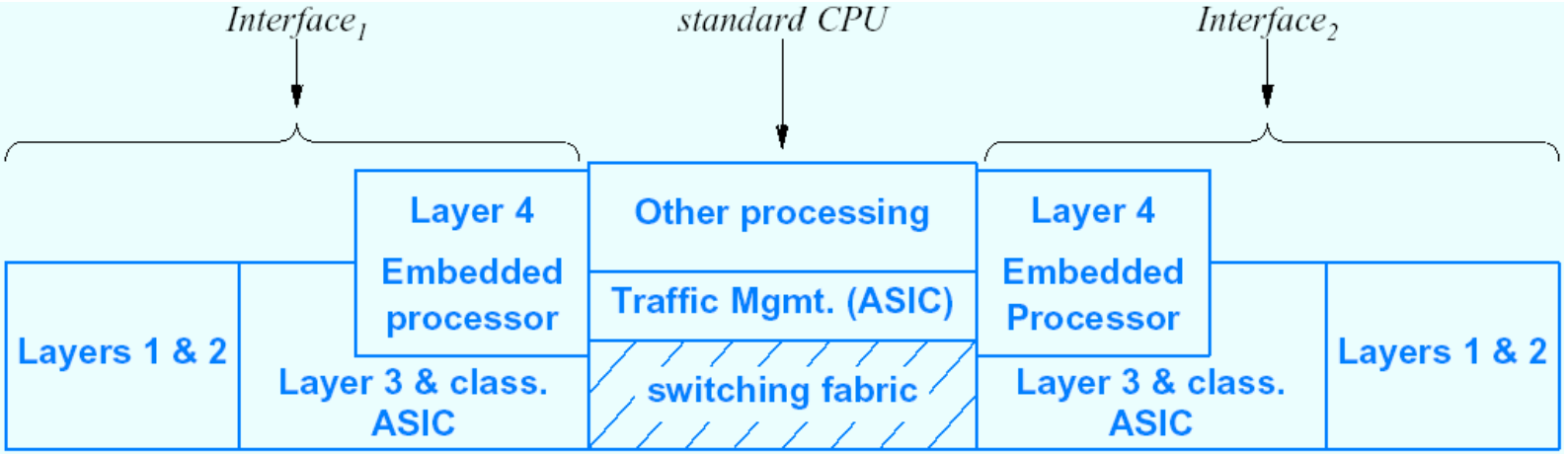


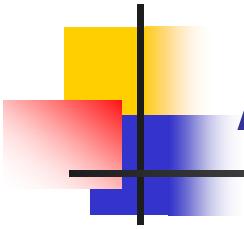
Outline

- Recap
  - Second generation network systems
  - Third generation network systems
  - Fourth generation network systems
- Complexity of network processor design
- Summary and homework

Various Architectures



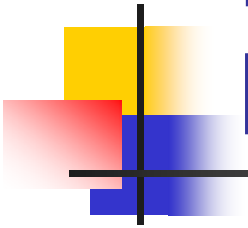




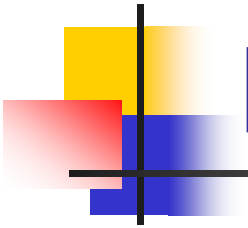
A Fourth Generation

- Goal: combine best features of first, second generation and third generation systems
  - Flexibility of programmable processor
  - High speed of ASICs
- Technology called *network processors*
  - A network processor is a special-purpose, programmable hardware device that combines the low cost and flexibility of a RISC processor with the speed and scalability of custom silicon (i.e., ASIC chips). Network processors are building blocks used to construct network systems.

How Should a Network Processor be Designed?

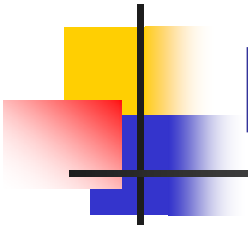


- Depends on
  - Operations network processor will perform
  - Role of network processor in overall system
- Generality
  - Sufficient for all protocols
  - Sufficient for all protocol processing tasks
  - Sufficient for all possible networks
- High speed
  - Scale to high bit rates
  - Scale to high packet rates



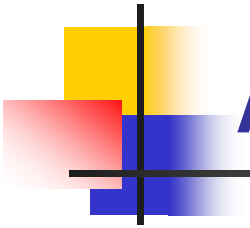
Key Points

- Elegance
  - Minimality, not merely comprehensiveness
- NOT designed to process a specific protocol or part of a protocol
- Seek a minimal set of instructions
  - Handle an arbitrary protocol processing task at high speed



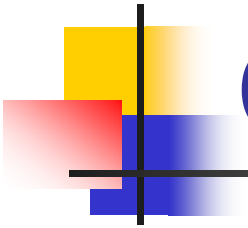
Functions We have Considered

- Address lookup and packet forwarding
- Error detection and correction
- Fragmentation, segmentation, & reassembly
- Frame and protocol demultiplexing
- Packet classification
- Queueing and packet discard
- Scheduling and timing
- Security: authentication and privacy
- Traffic measurement and policing
- Traffic shaping



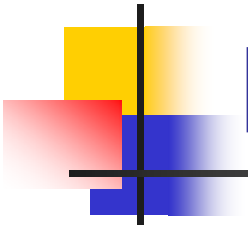
A Review Question

- Problem 1 of Chapter 12 (Page 183)



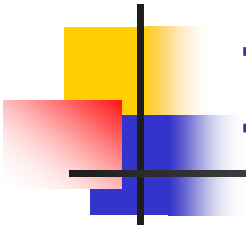
Questions

- Does our list of functions encompass all protocol processing?
- Which functions are most important to optimize?
- How do the functions map onto hardware units in a typical network system?
- Which hardware units in a network system can be replaced with network processors?
- What minimal set of instructions is sufficiently general to implement all functions?



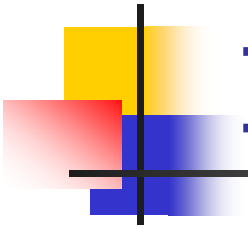
Division Of Functionality

- Partition problem to reduce complexity
  - Divide-and-conquer
- Basic division into two parts
  - Functions applied when packet arrives known as ingress processing
  - Functions applied when packet leaves known as egress processing



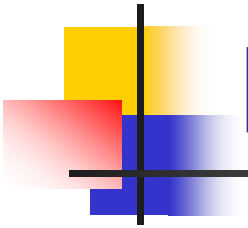
Ingress/Egress Processing

1. Addition of error detection codes
2. Address lookup and packet forwarding
3. Classification or demultiplexing
4. Forwarding, queueing, and scheduling
5. Header modification and/or transport splicing
6. Output security processing
7. Queueing and buffering
8. Reassembly or flow termination
9. Security and error detection
10. Segmentation or fragmentation
11. Timing and scheduling
12. Traffic measurement and policing
13. Traffic shaping (different from #12)



Ingress Processing

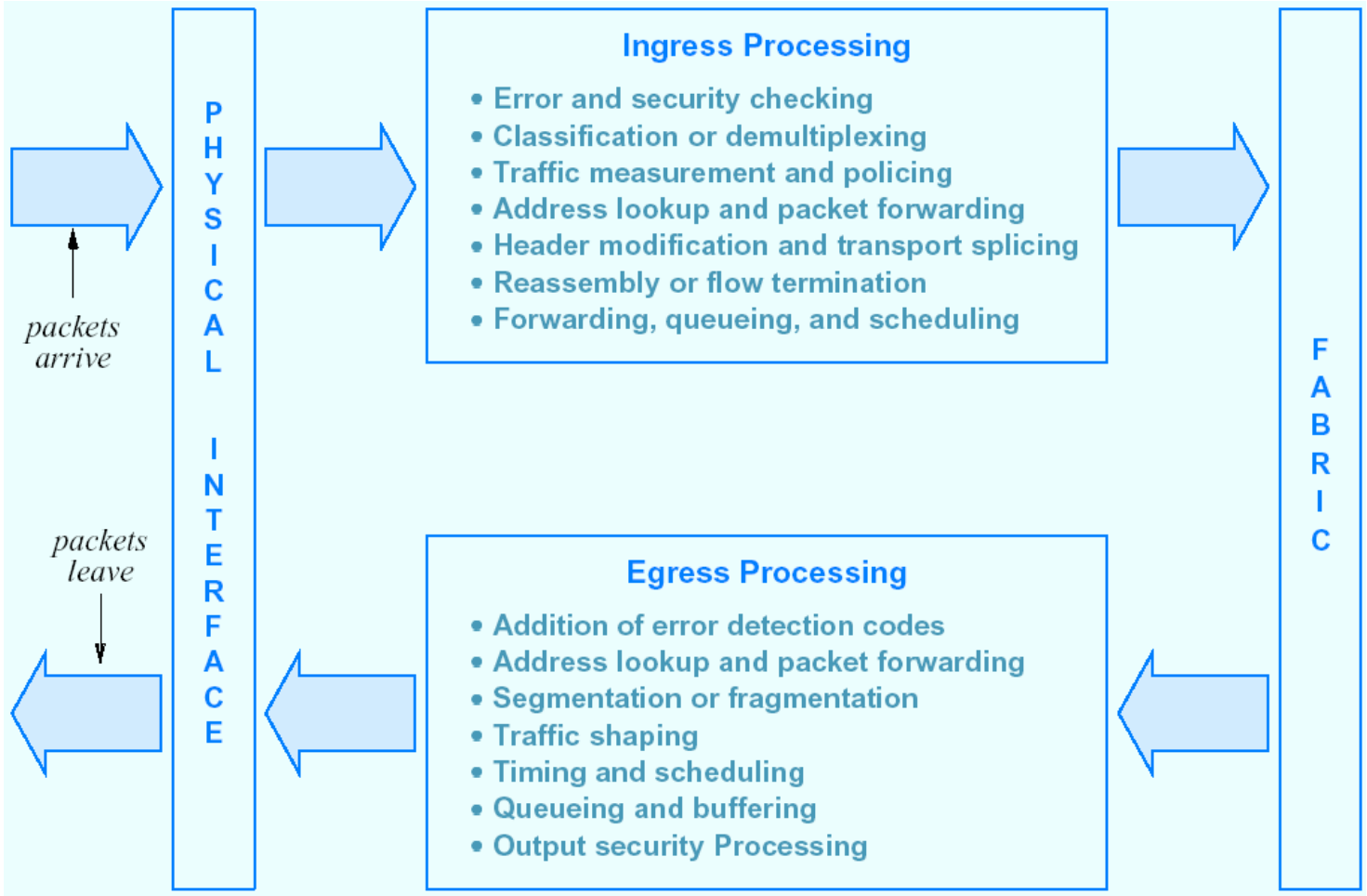
- Security and error detection
- Classification or demultiplexing
- Traffic measurement and policing
- Address lookup and packet forwarding
- Header modification and transport splicing
- Reassembly or flow termination
- Forwarding, queueing, and scheduling



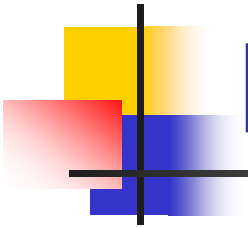
Egress Processing

- Addition of error detection codes
- Address lookup and packet forwarding
- Segmentation or fragmentation
- Traffic shaping
- Timing and scheduling
- Queueing and buffering
- Output security processing

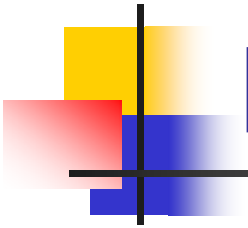
Illustration of Packet Flow



How will Network Processors be Used?

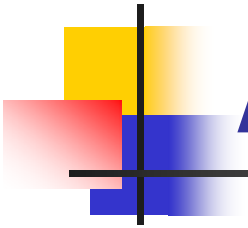


- For ingress processing only?
- For egress processing only?
- For combination?
- Architectural roles: everywhere?
  - Replacement for a conventional CPU
  - Augmentation of a conventional CPU
  - Input/output path of a NIC
  - Between a switching fabric and a NIC
  - Attach to a switching fabric



Replacing a Conventional CPU

- Both conventional and special instruction sets
  - Arithmetic manipulations
  - Access memory
  - Parse headers
  - Linked data structure with pointers
  - Floating point computation
  - Special instructions to manipulate packets

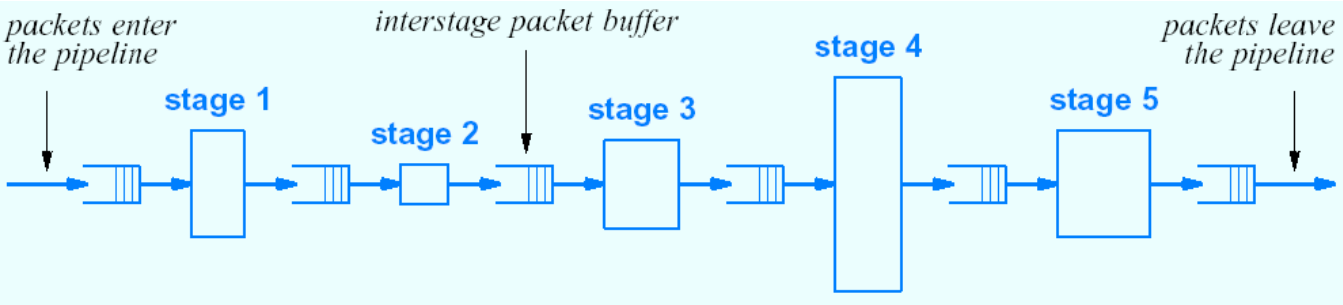


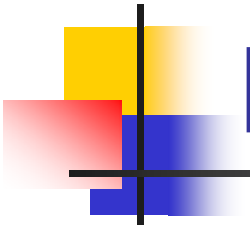
Augmenting Conventional CPU

- Pre-processing
- Co-processing
- Post-processing

How will Network Processors be Used?

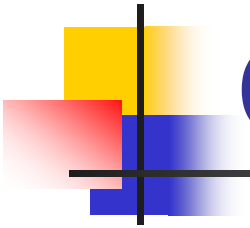
- Other architectural
  - Input/output path of a NIC
  - Between a switching fabric and a NIC
  - Attach to a switching fabric
- Scalability
  - Parallelism
  - Pipelining





Design by Software Emulation

- Hardware related
  - A chicken-and-egg problem
- Agere SPA network processor simulator



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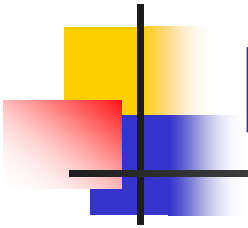

Homework (due on 03/28)

- 9.1 Individual lab report of Lab #3.
- 9.2 Problem 7 of Chapter 12 (Page 175)