

Michael F. Spear

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EDUCATION	University of Rochester , Rochester, New York USA Ph.D., Computer Science, August 2009 Dissertation Topic: “Fast Software Transactions” Advisor: Michael Scott M.S., Computer Science, December 2005 University of Alaska, Anchorage , Anchorage, Alaska USA Masters of Business Administration, May 2003 United States Military Academy , West Point, New York USA B.S., Computer Science, May 1999	
PROFESSIONAL EXPERIENCE	Lehigh University , Bethlehem, Pennsylvania USA Assistant Professor, Computer Science and Engineering	(8/09 – Present)
	University of Rochester , Rochester, New York Research Assistant, Department of Computer Science	(8/04 – 7/09)
	IBM T.J. Watson Research Center , Yorktown Heights, New York Research Intern	(05/07 – 08/07)
	Microsoft Research , Redmond, Washington Research Intern, Operating Systems Group	(06/05 – 08/05)
	Little Rock Air Force Base , Little Rock, Arkansas Executive Officer, 314th Maintenance Group Managed administration and automation for 1,300-person aircraft maintenance unit. Ranks held: First Lieutenant, Captain.	(12/02 – 07/04)
	Elmendorf Air Force Base , Anchorage, Alaska Assistant Chief of Wing Programs, 3rd Wing Led projects with 3-8 developers, integrating legacy databases and designing executive decision systems to deliver mission-critical data through web-based interfaces. Ranks held: Second Lieutenant, First Lieutenant.	(06/99 – 11/02)
RESEARCH INTERESTS	Exploiting parallelism and simplifying the development of correct multithreaded applications. Current efforts focus on transactional memory, lock-free data structures, and speculative parallelization of sequential code.	
PUBLICATIONS	Journal Publications (2) 1. “A Transactional Memory with Automatic Performance Tuning”, by Qingping Wang, Sameer Kulkarni, John Cavazos, and Michael Spear. In <i>ACM Transactions on Architecture and Code Optimization</i> 8(4): 54.1–54.23, 2012. Also appeared in proceedings of the 7th International Conference on High-Performance and Embedded Architectures and Compilers, Paris, France, January 2012.	

2. “Compiler and Runtime Techniques for Software Transactional Memory Optimization”, by Peng Wu, Maged Michael, Christoph von Praun, Takuya Nakaike, Rajesh Bordawekar, Harold Cain, Calin Cascaval, Siddhartha Chatterjee, Stefanie Chiras, Rui Hou, Mark Mergen, Xiaowei Shen, Michael Spear, Huayong Wang, and Kun Wang. In *Concurrency and Computation: Practice and Experience 21(1): 7-23*, 2009.

Refereed Conference Proceedings (17)

1. “Hybrid NOrec: A Case Study in the Effectiveness of Best Effort Hardware Transactional Memory”, by Luke Dalessandro, Francois Carouge, Sean White, Yossi Lev, Mark Moir, Michael Scott, and Michael Spear. In *Proceedings of the 16th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Newport Beach, CA, March 2011.
2. “A Scalable Lock-Free Universal Construction with Best Effort Transactional Hardware”, by Francois Carouge and Michael Spear. In *Proceedings of the 2010 International Symposium on DIStributed Computing (DISC)*, Cambridge, MA, September 2010.
3. “Transactions as the Foundation of a Memory Consistency Model”, by Luke Dalessandro, Michael Scott, and Michael Spear. In *Proceedings of the 2010 International Symposium on DIStributed Computing (DISC)*, Cambridge, MA, September 2010.
4. “Transactional Mutex Locks”, by Luke Dalessandro, Dave Dice, Michael Scott, Nir Shavit, and Michael Spear. In *Proceedings of the Euro-Par 2010 Conference (EuroPar 2010)*, Naples, Italy, August 2010.
5. “Robust, Lightweight Adaptivity for Software Transactional Memory”, by Michael Spear. In *Proceedings of the 22nd ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, Santorini, Greece, June 2010.
6. “NOrec: Streamlining STM by Abolishing Ownership Records”, by Luke Dalessandro, Michael Spear, and Michael Scott. In *Proceedings of the 15th ACM Symposium on Principles and Practice of Parallel Programming (PPoPP)*, Bangalore, India, January 2010.
7. “Reducing Memory Ordering Overheads in Software Transactional Memory”, by Michael Spear, Maged Michael, Michael Scott, and Peng Wu. In *Proceedings of the 2009 International Symposium on Code Generation and Optimization (CGO)*, Seattle, WA, March 2009.
8. “A Comprehensive Strategy for Contention Management in Software Transactional Memory”, by Michael Spear, Luke Dalessandro, Virendra Marathe, and Michael Scott. In *Proceedings of the 14th ACM Symposium on Principles and Practice of Parallel Programming (PPoPP)*, Raleigh, NC, February 2009.
9. “Ordering-Based Semantics for Software Transactional Memory”, by Michael Spear, Luke Dalessandro, Virendra Marathe, and Michael Scott. In *Proceedings of the 12th International Conference On Principles Of DIstributed Systems (OPODIS)*, Luxor, Egypt, December 2008.
10. “Implementing and Exploiting Inevitability in Software Transactional Memory”, by Michael Spear, Michael Silverman, Luke Dalessandro, Maged Michael, and Michael Scott. In *Proceedings of the 37th International Conference on Parallel Processing (ICPP)*, Portland, OR, September 2008.
11. “Scalable Techniques for Transparent Privatization in Software Transactional Memory”, by Virendra Marathe, Michael Spear, and Michael Scott. In *Proceedings of the 37th International Conference on Parallel Processing (ICPP)*, Portland, OR, September 2008.
12. “RingSTM: Scalable Transactions with a Single Atomic Instruction”, by Michael Spear, Maged Michael and Christoph von Praun. In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, Munich, Ger-

- many, June 2008.
13. “Delaunay Triangulation with Transactions and Barriers”, by Michael Scott, Michael Spear, Luke Dalessandro, and Virendra Marathe. In *Proceedings of the IEEE International Symposium on Workload Characterization (IISWC), Benchmarks track*, Boston, MA, September 2007.
 14. “An Integrated Hardware-Software Approach to Flexible Transactional Memory”, by Arrvindh Shriraman, Michael Spear, Hemayet Hossain, Virendra Marathe, Sandhya Dwarkadas, and Michael Scott. In *Proceedings of the 34th International Symposium on Computer Architecture (ISCA)*, San Diego, CA, June 2007. Earlier but expanded version available as *TR 910, Department of Computer Science, University of Rochester*, December 2006.
 15. “Nonblocking Transactions Without Indirection Using Alert-on-Update”, by Michael F. Spear, Arrvindh Shriraman, Luke Dalessandro, Sandhya Dwarkadas, and Michael L. Scott. In *Proceedings of the 19th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, San Diego, CA, June 2007.
 16. “Conflict Detection and Validation Strategies for Software Transactional Memory”, by Michael F. Spear, Virendra J. Marathe, William N. Scherer III, and Michael L. Scott. In *Proceedings of the 20th International Symposium on Distributed Computing (DISC)*, Stockholm, Sweden, September 2006.
 17. “Solving the Starting Problem: Device Drivers as Self-Describing Artifacts”, by Michael F. Spear, Tom Roeder, Orion Hodson, Galen Hunt, and Steven Levi. In *Proceedings of the EuroSys2006 Conference*, Leuven, Belgium, April 2006.

Refereed Workshop Proceedings (9)

1. “Toxic Transactions”, by Yujie Liu and Michael Spear. In *Proceedings of the 6th ACM SIGPLAN Workshop on Transactional Computing (TRANSACT)*, San Jose, CA, June 2011.
2. “Towards Applying Machine Learning to Adaptive Transactional Memory”, by Qingping Wang, Sameer Kulkarni, John Cavazos, and Michael Spear. In *Proceedings of the 6th ACM SIGPLAN Workshop on Transactional Computing (TRANSACT)*, San Jose, CA, June 2011.
3. “On Reconciling Hardware Atomicity, Memory Models, and `_tm_waiver`”, by Sean White and Michael Spear. In *Proceedings of the 2nd Workshop on the Theory of Transactional Memory (WTTM2010)*, Cambridge, MA, September 2010.
4. “Fastpath Speculative Parallelization”, by Michael Spear, Kirk Kelsey, Tongxin Bai, Luke Dalessandro, Michael Scott, Chen Ding, and Peng. Wu. In *Proceedings of the 22nd International Workshop on Languages and Compilers for Parallel Computing (LCPC)*, Newark, DE, October 2009.
5. “Transactional Mutex Locks”, by Michael Spear, Arrvindh Shriraman, Luke Dalessandro, and Michael Scott. In *Proceedings of the 4th ACM SIGPLAN Workshop on Transactional Computing (TRANSACT)*, Raleigh, NC, February 2009.
6. “Inevitability Mechanisms for Software Transactional Memory”, by Michael Spear, Maged Michael, and Michael Scott. In *Proceedings of the 3rd ACM SIGPLAN Workshop on Transactional Computing (TRANSACT)*, Salt Lake City, UT, February 2008.
7. “Capabilities and Limitations of Library-Based Software Transactional Memory in C++”, by Luke Dalessandro, Virendra Marathe, Michael Spear, and Michael Scott. In *Proceedings of the 2nd ACM SIGPLAN Workshop on Transactional Computing (TRANSACT)*, Portland, OR, August 2007.
8. “Lowering the Overhead of Software Transactional Memory”, by Virendra J. Marathe, Michael F. Spear, Christopher Heriot, Athul Acharya, David Eisenstat, William N. Scherer III, and Michael L. Scott. In *Proceedings of the 1st ACM SIGPLAN Workshop on Transactional Computing (TRANSACT)*, Ottawa, ON, Canada, June 2006. Earlier but expanded version available as *TR 893, Depart-*

- ment of Computer Science, University of Rochester, March 2006.
9. “Hardware Acceleration of Software Transactional Memory”, by Arrvindh Shriraman, Virendra J. Marathe, Sandhya Dwarkadas, Michael L. Scott, David Eisenstat, Christopher Heriot, William N. Scherer III, and Michael F. Spear. In *Proceedings of the 1st ACM SIGPLAN Workshop on Transactional Computing (TRANSACT)*, Ottawa, ON, Canada, June 2006.

Refereed Brief Announcements and Posters (8)

1. “A Lock-Free, Array-Based Priority Queue (POSTER)”, by Yujie Liu and Michael Spear. In *Proceedings of the 17th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP)*, New Orleans, LA, February 2012. To Appear.
2. “Brief Announcement: A Nonblocking Set Optimized for Querying the Minimum Value”, by Yujie Liu and Michael Spear. In *Proceedings of the 30th ACM Symposium on Principles of Distributed Computing (PODC)*, San Jose, CA, June 2011. Expanded version available as *TR LU-CSE-11-001, Computer Science and Engineering Department, Lehigh University*, May 2011.
3. “Hybrid TM Using NOrec STM (POSTER)”, by Luke Dalessandro, Michael Spear, and Michael Scott. In *Proceedings of the 15th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Pittsburgh, PA, March 2010.
4. “Transactional Memory Retry Mechanisms (brief announcement)”, by Michael Spear, Andrew Sveikauskas, and Michael Scott. In *Proceedings of the 27th ACM Symposium on Principles of Distributed Computing (PODC)*, Toronto, ON, Canada, August 2008. Expanded version available as *TR 935, Department of Computer Science, University of Rochester*, June 2008.
5. “Transaction Safe Nonblocking Data Structures (brief announcement)”, by Virendra Marathe, Michael Spear and Michael Scott. In *Proceedings of the 21st International Symposium on Distributed Computing (DISC)*, Lemesos, Cyprus, September 2007.
6. “Privatization Techniques for Software Transactional Memory (brief announcement)”, by Michael Spear, Virendra Marathe, Luke Dalessandro, and Michael Scott. In *Proceedings of the 26th ACM Symposium on Principles of Distributed Computing (PODC)*, Portland, OR, August 2007. Expanded version available as *TR 915, Department of Computer Science, University of Rochester*, February 2007.
7. “Transactions and Privatization in Delaunay Triangulation (brief announcement)”, by Michael Scott, Michael Spear, Luke Dalessandro, and Virendra Marathe. In *Proceedings of the 26th ACM Symposium on Principles of Distributed Computing (PODC)*, Portland, OR, August 2007.
8. “Alert-on-Update: A Communication Aid for Shared Memory Multiprocessors (poster paper)”, by Michael F. Spear, Arrvindh Shriraman, Hemayet Hossain, Sandhya Dwarkadas, and Michael L. Scott. In *Proceedings of the 12th ACM Symposium on Principles and Practice of Parallel Programming (PPoPP)*, San Jose, CA, March 2007.

Working Papers (5)

1. “Delegation and Nesting in Best Effort Transactional Memory”. With Yujie Liu and Stephan Diestelhorst (AMD). To be submitted to ACM SPAA 2012.
2. “A Nonblocking Set Optimized for Querying the Minimum Value”. With Yujie Liu. To be submitted to ACM PODC 2012.
3. “On the Use of Performance Counters in Adaptive Transactional Memory”. With John Cavazos (U. Delaware). In preparation.

4. “Design to Combine: Scalable Tree-Based Algorithms for Combining Synchronization”. With Yujie Liu. In preparation.
5. “Biased Transactions”. With Wenjia Ruan. In preparation.

Patents Pending (4)

1. Christoph von Praun and Michael Spear, “Architectural Support for Software Thread-Level Speculation”.
2. Maged Michael, Michael Spear, and Christoph von Praun, “Managing Concurrent Transactions Using Bloom Filters”.
3. Galen C Hunt, James R Larus, Orion Hodson, Steven P Levi, Bjarne Steensgaard, David R Tarditi, Manuel A Fahndrich, Michael Spear, and Michael Carbin, “Configuration of Isolated Extensions and Device Drivers”.
4. Michael Scott, Sandhya Dwarkadas, Arrvindh Shriraman, Virendra Marathe, and Michael Spear, “System and Method for Hardware Acceleration of a Software Transactional Memory”.

HONORS AND AWARDS

- P.C. Rossin Assistant Professorship, 2011-2013.
- Outstanding Dissertation Award (Engineering), University of Rochester, 2010
- 3rd Wing Staff Officer of the Year, 2000
- U.S. Grant Award (top graduate in Computer Science at West Point), 1999
- USMA Distinguished Graduate, 1999

RESEARCH GRANTS

Competitively Awarded Research Grants

- (PI) National Science Foundation, Computer and Network Systems, “CSR: Small: Adaptive Synchronization for Multicore Systems”. Aug 2010 – Jul 2013, \$250,025. CNS-1016828.
- (PI) Google, “Lock-Free Linux By Refinement”. Feb 2012 – Feb 2013, \$46,000. (Additional proposals under review.)

Non-Competitive Grants

- (PI) National Science Foundation, Computing and Communication Foundations, “Student Travel Support for the 16th ACM SIGPLAN Annual Symposium on Principles and Practice of Parallel Programming (PPoPP 2011)”. Jul 2010 – Jun 2011, \$10,000. CCF-1044312.
- Laboratory Enhancement Grant, P.C. Rossin College of Engineering and Applied Science, Lehigh University, 2011.

PROFESSIONAL PRESENTATIONS

Invited Talks (2)

1. “Adaptivity in Software Transactional Memory”, University of Delaware, May 2010.
2. “Job Hunting in a Tight Market”, 2009 SOSP Diversity Workshop, Big Sky, MT, October 2009.

Refereed Presentations (9)

1. “Towards Applying Machine Learning to Adaptive Transactional Memory”, ACM SIGPLAN Workshop on Transactional Computing, San Jose, CA, June 2011.
2. “Robust, Lightweight Adaptivity for Software Transactional Memory”, ACM Symposium on Parallelism in Algorithms and Architectures, Santorini, Greece, June 2010.
3. “Reducing Memory Ordering Overheads in Software Transactional Memory”, International Symposium on Code Generation and Optimization, Seattle, Washington, March 2009.

4. "A Comprehensive Strategy for Contention Management in Software Transactional Memory", ACM Symposium on Principles and Practice of Parallel Programming, Raleigh, North Carolina, February 2009.
5. "Transactional Mutex Locks", ACM SIGPLAN Workshop on Transactional Computing, Raleigh, North Carolina, February 2009.
6. "Inevitability Mechanisms for Software Transactional Memory", ACM SIGPLAN Workshop on Transactional Computing, Salt Lake City, Utah, February 2008.
7. "Nonblocking Transactions Without Indirection Using Alert-on-Update", ACM Symposium on Parallelism in Algorithms and Architectures, San Diego, California, June 2007.
8. "Lowering the Overhead of Software Transactional Memory", 1st ACM SIGPLAN Workshop on Transactional Computing (TRANSACT), Ottawa, Ontario, Canada, June 2006.
9. "Solving the Starting Problem: Device Drivers as Self-Describing Artifacts", EuroSys 2006 Conference, Leuven, Belgium, April 2006.

TEACHING &
ADVISING

Courses Taught (8)

1. Spring 2012: CSE 398 Xtreme Projects: Mobile Programming (20 Undergraduate, 3 Graduate)
2. Spring 2012: CSE 403 Theory of Operating Systems (9 Graduate)
3. Fall 2011: CSE 375 Hardware and Software Topics in Parallel Computing (9 Undergraduate, 12 Graduate)
4. Fall 2011: Engr 98 Introduction to Engineering Practice: Computer Engineering Project (50 Undergraduate)
5. Spring 2011: CSE 403 Theory of Operating Systems (2 Undergraduate, 15 Graduate)
6. Fall 2010: CSE 201/ECE 201 Computer Architecture (22 Undergraduate)
7. Spring 2010: CSE 375/CSE 498 Hardware and Software Topics in Parallel Computing (6 Undergraduate, 17 Graduate)
8. Fall 2009: CSE 201/ECE 201 Computer Architecture (18 Undergraduate)

SERVICE

University Service

Computer Science and Engineering Department, Lehigh University

- Computer Facilities, 2011-present
- Publicity and Web, 2011-present
- Admissions Committee, 2009-2011
- PhD Qualifier Committee, 2009-2011
- PhD Program Review Committee, 2010-2011
- Lehigh-USMA CS Graduate Partnership, 2010-present

Lehigh University

- High Performance Computing Steering Committee, 2010-present
- Faculty Athletics Committee, 2011-present

Professional Activities

Conference Committees

- Program Committee, 5th ACM Workshop on Transactional Computing
- Program Committee, 22nd ACM Symposium on Parallelism in Algorithms and Architectures
- Registration Chair and External Review Committee, 16th ACM Symposium on Principles and Practice of Parallel Programming
- Program Committee, Algorithms Track, 2011 International Conference on Distributed Computing Systems

- Program Committee, 6th ACM Workshop on Transactional Computing
- Program Committee, 25th International Symposium on Distributed Computing
- External Review Committee, 17th ACM Symposium on Principles and Practice of Parallel Programming
- Co-chair, 2011 Workshop on Wild and Sane Ideas in Speculation and Transactions
- Chair, 2012 ACM SIGPLAN Workshop on Transactional Computing
- Program Committee, 2012 ACM SIGPLAN International Symposium on Memory Management

Outside Reviewer

- IEEE International Parallel & Distributed Processing Symposium (2010)
- International Symposium on High-Performance Computer Architecture (2010)
- Journal of Parallel and Distributed Computing (2010, 2011)
- ACM SIGACT-SIGOPS Symposium on Principles of Distributed Computing (2010)
- IEEE Computer Architecture Letters (2010, 2011)
- International Conference on Parallel Architectures and Compilation Techniques (2010)
- Concurrency and Computation: Practice and Experience (2011)
- Distributed Computing (2011)
- IEEE Transactions on Parallel and Distributed Systems (2011)
- International Workshop on Languages and Compilers for Parallel Computing (2011)
- ACM Transactions on Programming Languages and Systems (2011)
- ACM Transactions on Computer Systems (2012)